Puma (microarchitecture)

The **Puma Family 16h** is a low-power microarchitecture by AMD for its APUs. It succeeds the Jaguar as a second-generation version, targets the same market, and belongs to the same AMD architecture Family 16h. The *Beema* line of processors are aimed at low-power notebooks, and *Mullins* are targeting the tablet sector.

Puma - Family 16h (2nd-gen)

General information	
Launched	mid-2014
Discontinued	mid-2015
Common manufacturer(s)	AMD
Performance	
Max. CPU clock rate	1.35 GHz to 2.5 GHz
Cache	
L1 cache	64 KB per core[1]
L2 cache	1 MB to 2 MB shared
Architecture and classification	
Technology node	28 nm
Instruction set	AMD64 (x86-64)
Physical specifications	
Cores	2–4
GPU(s)	Radeon Rx: 128 cores, 300–800 Mhz
Socket(s)	Socket AM1 Socket FT3b (BGA-769)
Products, models, variants	
Core name(s)	Beema Mullins
Brand name(s)	AMD APU
History	
Predecessor(s)	Jaguar - Family 16h

Design

The Puma cores use the same microarchitecture as Jaguar, and inherits the design:

- Out-of-order execution and Speculative execution, up to 4 CPU cores
- Two-way integer execution
- Two-way 128-bit wide floating-point and packed integer execution
- Integer hardware divider
- Puma **does not** feature clustered multi-thread (CMT), meaning that there are no "modules"
- Puma **does not** feature Heterogeneous System Architecture or zero-copy[2]
- 32 KiB instruction + 32 KiB data L1 cache per core
- 1–2 MiB unified L2 cache shared by two or four cores
- Integrated single channel memory controller supporting 64bit DDR3L
- 3.1 mm^2 area per core

Instruction set support

Like Jaguar, the *Puma* core has support for the following instruction sets and instructions: MMX, SSE, SSE2, SSE3, SSSE3, SSE4a, SSE4.1, SSE4.2, AVX, F16C, CLMUL, AES, BMI1, MOVBE (Move Big-Endian instruction), XSAVE/XSAVEOPT, ABM (POPCNT/LZCNT), and AMD-V.[1]

Improvements over *Jaguar*

- 19% CPU core leakage reduction at 1.2V[3]
- 38% GPU leakage reduction
- 500 mW reduction in memory controller power
- 200 mW reduction in display interface power
- Chassis temperature aware turbo boost[4]
- Selective boosting according to application needs (intelligent boost)
- Support for ARM TrustZone via integrated Cortex-A5 processor
- Support for DDR3L-1866 memory[5]

Puma+

AMD released a revision of Puma microarchitecture, Puma+, updating the video decoder from UVD 4.2 to 6.0 and the video encoder from VCE 2.0 to VCE 3.1.

Features

APU features table

Processors

Desktop/Mobile (Beema)

Family	Model	Socket	CPU				GPU			TDP (W)	DDR3L Memory Speed
			Cores	Freq. (GHz)	Max. Turbo (GHz)	L2 Cache (MB)	Model	Config.	Max. Freq. (MHz)		
A8	6410	Socket FT3b	4	2.0	2.4	2	Radeon R5	128:?:?	800	15	1866
A6	6310			1.8			Radeon R4				
A4	6250J			2.0	—		Radeon R3		600	25	1600
A4	6210			1.8			Radeon R3			15	
E2	6110			1.5			Radeon R2		500		
E1	6010		2	1.35		1			350	10	1333

Tablet (Mullins)

Family	Model	CPU				GPU			Power		DDR3L Memory Speed
		Cores	Freq. (GHz)	Max. Turbo (GHz)	L2 Cache (MB)	Model	Config.	Max. Freq. (MHz)	TDP (W)	SDP (W)	
A10 Micro	6700T	4	1.2	2.2	2	Radeon R6	128:?:?	500	4.5	2.8	1333
A6 Micro	6500T			1.8		Radeon R4		401			
A4 Micro	6400T		1.0	1.6		Radeon R3		350			
E1 Micro	6200T	2		1.4	1	Radeon R2		300	3.95		1066

References

1. "Software Optimization Guide for Family 16h Processors" (http://support.amd.com/TechDocs/52128_16h_Software_Opt_Guide.zip). AMD. Retrieved August 3, 2013.
2. "AMD launches new Beema, Mullins SoCs" (http://www.extremetech.com/computing/181407-amd-launches-new-beema-mullins-socs-higher-performance-at-almost-low-enough-tdps). *ExtremeTech*. 2014-04-29. Retrieved 2014-05-02.
3. Shimpi, Anand. "AMD Beema/Mullins Architecture & Performance Preview" (http://anandtech.com/show/7974/amd-beema-mullins-architecture-a10-micro-6700t-performance-preview). AnandTech. Retrieved 29 April 2014.
4. Shimpi, Anand. "New Turbo Boost, The Lineup and Trustzone" (http://anandtech.com/show/7974/amd-beema-mullins-architecture-a10-micro-6700t-performance-preview/2). AnandTech. Retrieved 29 April 2014.

5. Woligroski, Don (28 April 2014). "Meet The Mullins And Beema Tablet APUs" (http://www.tomshardware.com/reviews/amd-tablet-processor,3813.html). Toms Hardware. Retrieved 29 April 2014.

External links

- Software Optimization Guide for Family 16h Processors (http://support.amd.com/TechDocs/52128_16h_Software_Opt_Guide.zip)
- 2014 AMD Low-Power Mobile APUs (https://www.slideshare.net/AMD/2014-amd-lowpower-mobile-apus)
- Jaguar presentation (video) (https://player.vimeo.com/video/70360819) at ISSCC 2013
- Discussion initiated on RWT forums by Jeff Rupley, Chief Architect of the Jaguar core (http://www.realworldtech.com/forum/?threadid=132914)
- BKDG for Family 16h Models 00h-0Fh Processors (http://support.amd.com/TechDocs/48751_16h_bkdg.pdf)
- Revision Guide for Family 16h Models 00h-0Fh Processors (http://support.amd.com/TechDocs/51810_16h_00h-0Fh_Rev_Guide.pdf) (Jaguar)
- Revision Guide for Family 16h Models 30h-3Fh Processors (http://support.amd.com/TechDocs/53072_Rev_Guide_16h_Models_30h-3Fh.pdf) (Puma)