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ARM9

ARM9 is a group of 32-bit RISC ARM processor cores licensed by ARM Holdings for microcontroller use.[1] The ARM9 core family consists of ARM9TDMI, ARM940T, ARM9E-S, ARM966E-S, ARM920T, ARM922T, ARM946E-S, ARM9EJ-S, ARM926EJ-S, ARM968E-S, ARM996HS. ARM9 cores were released from 1998 to 2006 and they are no longer recommended for new IC designs; recommended alternatives include ARM Cortex-A, ARM Cortex-M, and ARM Cortex-R cores.

ARM9T

General information	
Designed by	ARM Holdings
Architecture and classification	
Microarchitecture	ARMv4T
Instruction set	ARM (32-bit), Thumb (16-bit)

ARM9E

Performance	
Max. CPU clock rate	100 MHz to 600 MHz
Architecture and classification	
Microarchitecture	ARMv5TE
Instruction set	ARM (32-bit), Thumb (16-bit)

ARM9EJ

Architecture and classification	
Microarchitecture	ARMv5TEJ
Instruction set	ARM (32-bit), Thumb (16-bit), Jazelle (8-bit)

Overview

With this design generation, ARM moved from a von Neumann architecture (Princeton architecture) to a (modified; meaning split cache) Harvard architecture with separate instruction and data buses (and caches), significantly increasing its potential speed.[2] Most silicon chips integrating these cores will package them as modified Harvard architecture chips, combining the two address buses on the other side of separated CPU caches and tightly coupled memories.

There are two subfamilies, implementing different ARM architecture versions.

Differences from ARM7 cores

Key improvements over ARM7 cores, enabled by spending more transistors, include:[3]

- Decreased heat production and lower overheating risk.
- Clock frequency improvements. Shifting from a three-stage pipeline to a five-stage one lets the clock speed be approximately doubled, on the same silicon fabrication process.
- Cycle count improvements. Many unmodified ARM7 binaries were measured as taking about 30% fewer cycles to execute on ARM9 cores. Key improvements include:
  - Faster loads and stores; many instructions now cost just one cycle. This is helped by both the modified Harvard architecture (reducing bus and cache contention) and the new pipeline stages.
  - Exposing pipeline interlocks, enabling compiler optimizations to reduce blockage between stages.

Additionally, some ARM9 cores incorporate "Enhanced DSP" instructions, such as a multiply-accumulate, to support more efficient implementations of digital signal processing algorithms.

Switching from a von Neumann architecture entailed using a non-unified cache, so that instruction fetches do not evict data (and vice versa). ARM9 cores have separate data and address bus signals, which chip designers use in various ways. In most cases they connect at least part of the address space in von Neumann style, used for both instructions and data, usually to an AHB interconnect connecting to a DRAM interface and an External Bus Interface usable with NOR flash memory. Such hybrids are no longer pure Harvard architecture processors.

ARM license

ARM Holdings neither manufactures nor sells CPU devices based on its own designs, but rather licenses the processor architecture to interested parties. ARM offers a variety of licensing terms, varying in cost and deliverables. To all licensees, ARM provides an integratable hardware description of the ARM core, as well as complete software development toolset and the right to sell manufactured silicon containing the ARM CPU.

Silicon customization

Integrated device manufacturers (IDM) receive the ARM Processor IP as synthesizable RTL (written in Verilog). In this form, they have the ability to perform architectural level optimizations and extensions. This allows the manufacturer to achieve custom design goals, such as higher clock speed, very low power consumption, instruction set extensions, optimizations for size, debug support, etc. To determine which components have been included in a particular ARM CPU chip, consult the manufacturer datasheet and related documentation.

Cores

The ARM MPCore family of multicore processors support software written using either the asymmetric (AMP) or symmetric (SMP) multiprocessor programming paradigms. For AMP development, each central processing unit within the MPCore may be viewed as an independent processor and as such can follow traditional single processor development strategies.[4]

Year	ARM9 Cores
1998	ARM9TDMI
1998	ARM940T
1999	ARM9E-S
1999	ARM966E-S
2000	ARM920T
2000	ARM922T
2000	ARM946E-S
2001	ARM9EJ-S
2001	ARM926EJ-S
2004	ARM968E-S
2006	ARM996HS

ARM9TDMI

ARM9TDMI is a successor to the popular ARM7TDMI core, and is also based on the ARMv4T architecture. Cores based on it support both 32-bit ARM and 16-bit Thumb instruction sets and include:

- ARM920T with 16 KB each of I/D cache and an MMU
- ARM922T with 8 KB each of I/D cache and an MMU
- ARM940T with cache and a Memory Protection Unit (MPU)

ARM9E-S and ARM9EJ-S

ARM9E, and its ARM9EJ sibling, implement the basic ARM9TDMI pipeline, but add support for the ARMv5TE architecture, which includes some DSP-esque instruction set extensions. In addition, the multiplier unit width has been doubled, halving the time required for most multiplication operations. They support 32-bit, 16-bit, and sometimes 8-bit instruction sets.

- ARM926EJ-S with ARM Jazelle technology, which enables the direct execution of 8-bit Java bytecode in hardware, and an MMU
- ARM946
- ARM966
- ARM968

The TI-Nspire CX (2011) and CX II (2019) graphing calculators use an ARM926EJ-S processor, clocked at 132 and 396 MHz respectively.[5]

Chips

ARM920T

- Atmel AT91RM9200[6]
- Cirrus Logic EP9315 ARM9 CPU, 200 MHz
- NXP i.MX1
- Samsung S3C2410, S3C2440, S3C2442, S3C2443

ARM922T

- Micrel/Kendin KS8695
- NXP LH7A4xx

ARM925T

- Texas Instruments OMAP 1510

ARM926EJ-S

- ASPEED AST2400
- Cypress Semiconductor EZ-USB FX3
- Microchip Technology (former Atmel) AT91SAM9260,[6] AT91SAM9G,[7] AT91SAM9M,[8] AT91SAM9N/CN,[9] AT91SAM9R/RL,[10] AT91SAM9X,[11] AT91SAM9XE[12] (see AT91SAM9)
- Nintendo Starlet (Wii coprocessor)[13]
- Nuvoton NUC900
- NXP (former Freescale Semiconductor) i.MX2 Series,[14] (see I.MX), LPC3100 and LPC3200 Series[15]
- Samsung S3C2412, S3C2416, S3C2450
- STMicroelectronics Nomadik
- Texas Instruments OMAP 850, 750, 733, 730, 5912 (also 5948, which is a customer specific version of it, made for Bosch), 1610
- Texas Instruments Sitara AM1x, OMAP L137/L138, Davinci DA830/DA850/DM355/DM365
- HP iLO 4[16] baseboard management controller
- 5V Technologies 5VT1310/1312/1314
- STMicroelectronics SPEAr300/600[17]
- VIA WonderMedia 8505 and 8650

ARM940T

- Conexant CX22490 STB SoC

ARM946E-S

- Nintendo NTR-CPU (Nintendo DS CPU), TWL-CPU (Nintendo DSi CPU; same as the DS but clocked at 133 MHz instead of 67 MHz)[18]
- NXP Nexperia PNX5230

ARM966E-S

- LSI Logic LSI53C1030
- STMicroelectronics STR9[19]

ARM968E-S

- NXP Semiconductors LPC2900

Unreferenced ARM9 core

- Anyka AK32xx
- Atmel AT91CAP9
- CSR Quatro 4300
- Centrality Atlas III
- Digi NS9215, NS9210[20]
- HiSilicon Kirin K3V1
- Infineon Technologies S-GOLDlite PMB 8875
- LeapFrog LF-1000
- NXP Semiconductors (former Freescale Semiconductor) i.MX1x
- MediaTek MT1000, MT6235-39, MT6268, MT6516
- PRAGMATEC RABBITV3 (ARM920T rev 0 (v4l)) used in Karotz)
- Qualcomm MSM6xxx
- Qualcomm Atheros AR6400
- Texas Instruments TMS320DM365/TMS320DM368 ARM9EJ-S
- Zilog Encore! 32

Nintendo DSi has a chip with an ARM9 and ARM7 core

Lego Mindstorms EV3 brick has an ARM9 TI Sitara AM1x

ARM946E-S baseband processor on a Samsung SGH-D900 phone

Samsung S3C2416XH-26

Documentation

The amount of documentation for all ARM chips is daunting, especially for newcomers. The documentation for microcontrollers from past decades would easily be inclusive in a single document, but as chips have evolved so has the documentation grown. The total documentation is especially hard to grasp for all ARM chips since it consists of documents from the IC manufacturer and documents from CPU core vendor (ARM Holdings).

A typical top-down documentation tree is: high-level marketing slides, datasheet for the exact physical chip, a detailed reference manual that describes common peripherals and other aspects of physical chips within the same series, reference manual for the exact ARM core processor within the chip, reference manual for the ARM architecture of the core which includes detailed description of all instruction sets.

Documentation tree (top to bottom)

1. IC manufacturer marketing slides.
2. IC manufacturer datasheets.
3. IC manufacturer reference manuals.
4. ARM core reference manuals.
5. ARM architecture reference manuals.

IC manufacturer has additional documents, including: evaluation board user manuals, application notes, getting started with development software, software library documents, errata, and more.

See also

- ARM architecture
- List of ARM architectures and cores
- JTAG
- Interrupt, Interrupt handler
- Real-time operating system, Comparison of real-time operating systems

Electronics portal

References

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8. SAM9M ARM9 Microcontrollers; Microchip. (http://www.atmel.com/products/microcontrollers/arm/sam9m.aspx)
9. SAM9N/CN ARM9 Microcontrollers; Atmel. (http://www.atmel.com/products/microcontrollers/arm/sam9n.aspx)
10. SAM9R/RL ARM9 Microcontrollers; Atmel. (http://www.atmel.com/products/microcontrollers/arm/sam9r.aspx)
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External links

ARM9 official documents

- ARM9 official website (http://www.arm.com/products/processors/classic/arm9/index.php)
- Architecture Reference Manual: ARMv4/5/6 (https://silver.arm.com/download/ARM_Architecture/AR550-DA-70002-r0p0-00rel0/DDI%2001001.pdf)
- Core Reference Manuals: ARM9E-S (http://infocenter.arm.com/help/topic/com.arm.doc.ddi0240b/DDI0240A.pdf), ARM9EJ-S (http://infocenter.arm.com/help/topic/com.arm.doc.ddi0222b/DDI0222.pdf),ARM9TDMI (http://infocenter.arm.com/help/topic/com.arm.doc.ddi0180a/DDI0180.pdf),ARM920T (http://infocenter.arm.com/help/topic/com.arm.doc.ddi0151c/ARM920T_TRM1_S.pdf),ARM922T (http://infocenter.arm.com/help/topic/com.arm.doc.ddi0184b/DDI0184.pdf),ARM926EJ-S (http://infocenter.arm.com/help/topic/com.arm.doc.ddi0198e/DDI0198E_arm926ejs_r0p5_trm.pdf),ARM940T (http://infocenter.arm.com/help/topic/com.arm.doc.ddi0144b/940T_TRM_S.pdf),ARM946E-S (http://infocenter.arm.com/help/topic/com.arm.doc.ddi0201d/DDI0201D_arm946es_r1p1_trm.pdf),ARM966E-S (http://infocenter.arm.com/help/topic/com.arm.doc.ddi0213e/ARM966E-S_TRM.pdf),ARM968E-S (http://infocenter.arm.com/help/topic/com.arm.doc.ddi0311d/DDI0311.pdf)
- Coprocessor Reference Manuals: VFP9-S (Floating-Point) (http://infocenter.arm.com/help/topic/com.arm.doc.ddi0238c/DDI0238C_vfp9s_r0p2_trm.pdf), MOVE (MPEG4) (http://infocenter.arm.com/help/topic/com.arm.doc.ddi0235c/DDI0235.pdf)

Quick Reference Cards

- Instructions: Thumb (1 (http://infocenter.arm.com/help/topic/com.arm.doc.qrc0006e/QRC0006_UAL16.pdf)), ARM and Thumb-2 (2 (http://infocenter.arm.com/help/topic/com.arm.doc.qrc0001m/QRC0001_UAL.pdf)), Vector Floating Point (3 (http://infocenter.arm.com/help/topic/com.arm.doc.qrc0007e/QRC0007_VFP.pdf))
- Opcodes: Thumb (1 (http://re-eject.gbadev.org/files/ThumbRefV2-beta.pdf), 2 (http://www.mechcore.net/files/docs/ThumbRefV2-beta.pdf)), ARM (3 (http://re-eject.gbadev.org/files/armref.pdf), 4 (http://www.mechcore.net/files/docs/armref.pdf)), GNU Assembler Directives 5 (http://re-eject.gbadev.org/files/GasARMRef.pdf).